

3. (Amended) The apparatus of claim 1, wherein the converting block is coupled to provide a signal having a fractional pulse density that is indicative of acceleration.

4. (Amended) The apparatus of claim 1, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

5. (Amended) The apparatus of claim 1, wherein the converting block is configured to integrate the sensed signal and provide a first output signal and a second output signal.

6. (Amended) The apparatus of claim 5, wherein the converting block is further configured to compare the first output signal and the second output signal and provide an output signal.

7. (Amended) The apparatus of claim 6, wherein the converting block is coupled to provide the output signal to the input block.

8. (Amended) The apparatus of claim 1, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

9. (Amended) The apparatus of claim 8, wherein the input block is coupled to provide the first input signal through the

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first capacitor and the second input signal through the second capacitor.

20. (Amended) The apparatus of claim 19, wherein the converting block is coupled to provide a digital signal based on the sensed signal.

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21. (Amended) The apparatus of claim 19, wherein the input block is coupled to apply a first signal to the common input terminal during a first clock phase and a second signal during a second clock phase.

22. (Amended) The apparatus of claim 19, wherein the input block comprises a first input capacitor and a second input capacitor, wherein the input block is coupled to provide a first input signal to the converting block through the first input capacitor and a second input signal to the converting block through the second input capacitor.

26. (Amended) The restraint system of claim 25, wherein the deployment block is coupled to provide the activation signal to activate an airbag.

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27. (Amended) The restraint system of claim 25, wherein the sensing circuit is coupled to be clocked via a plurality of non-overlapping clocks.

28. (Amended) The restraint system of claim 25, wherein the sensing circuit is configured to provide a digital signal.